

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Canceled).

Claim 2 (Currently Amended): ~~A matrix array substrate according to claim 1, said first connector electrode being comprised of;~~

A matrix array substrate comprising:

scanning lines arranged substantially in parallel;

signal lines arranged substantially perpendicular to the scanning lines;

pixel electrodes each arranged on a respective patch in a matrix formed by the scanning and signal lines;

a switching element disposed at or around an intersection of one of the scanning lines and one of the signal lines and configured to input a signal to a respective one of the pixel electrodes from said one signal line in accordance with an electric current on said one scanning line;

a storage-capacity-forming extended portion extended from a first one of the pixel electrodes towards a second one of the pixel electrodes, said first pixel electrode being interposed between first and second ones of the scanning lines and configured to be supplied with a signal in accordance with an applied current on the first scanning line, said second pixel electrode configured to be supplied with a signal in accordance with an applied current on the second scanning line, and said storage-capacity-forming extended portion overlapping the second scanning line with an insulator film therebetween;

a tandem repair circuit comprised of,

a first connector electrode connected with the storage-capacity-forming extended portion extended from the first pixel electrode,

a second connector electrode distanced from the first connector electrode and connected with said second pixel electrode,

a third connector electrode bridging over the first connector electrode to the second connector electrode, and

a contact hole passing through the insulator film and electrically connecting the first connector electrode to the storage-capacity-forming extended portion, said contact hole being placed within contours of said second scanning line;

a thin-width wiring portion extending from an area above said third connector electrode to an area above said one of scanning line and substantially perpendicularly crossing a contour of said one of scanning lines line; and

a thick-width wiring portion ~~being~~ connected with an end of said thin-width wiring portion and located within contours of said scanning lines.

Claim 3 (Currently Amended): A matrix array substrate according to claim ~~1~~ 2, said thick-width wiring portion having a size along the said one scanning line larger than a width of ~~the~~ said one scanning line.

Claim 4 (Currently Amended): A matrix array substrate according to claim ~~1~~ 3, wherein said size of the thick-width wiring portion is substantially equal ~~with~~ to a sum of a size of said contact hole and a margin ~~for absorbing~~ configured to absorb a deviation of alignment during patterning of said contact hole.

Claim 5 (Canceled).

Claim 6 (Currently Amended): A matrix array substrate according to claim ~~4~~ 2,
wherein said third connector electrode ~~being is~~ included in a first-layer metal pattern and
formed simultaneously with the scanning lines, and said first and second connector electrodes
~~being are~~ included in a second-layer metal pattern and formed simultaneously with the signal
lines.

Claim 7 (Currently Amended): A matrix array substrate according to claim 6,
wherein said second-layer metal pattern ~~being is~~ formed of aluminum metal or ~~its an~~
aluminum alloy.

Claim 8 (Currently Amended): A matrix array substrate according to claim ~~4~~ 6,
wherein said pixel electrodes and said storage-capacity-forming extended portions are
included in a pattern of transparent electric-conductive material, ~~which is~~ disposed in a layer
above said first- and second-layer metal ~~pattern~~ patterns.

Claim 9 (Original): A matrix array substrate comprising:
a first-layer wiring pattern including scanning lines and gate electrodes arranged on an
insulator substrate;
a gate insulator film covering the first-layer wiring pattern;
a second-layer wiring pattern including signal lines and source and drain electrodes;
light reflective pixel electrodes each being connected with respective one of the
source electrodes; and
a storage-capacity-forming extended portion being extended from first of the pixel
electrode towards second of the pixel electrode, said first pixel electrode being interposed
between first and second ones of the scanning lines and being supplied with a signal in

accordance with an applied current on the first scanning line, said second pixel electrode being supplied with a signal in accordance with an applied current on the second scanning line, and said storage-capacity-forming extended portion overlapping the second scanning line with an insulator film therebetween;

further comprising:

an island pattern being included in said second-layer wiring pattern and disposed within an overlapping area in which said storage-capacity-forming extended portion overlaps said second scanning line, and said island pattern having a size along said second scanning line larger than width of said second scanning line.

Claim 10 (Original): A matrix array substrate according to claim 9, further comprising:

a contact hole on an insulator film covering the island pattern, for electrically connecting with said storage-capacity-forming extended portion.

Claim 11 (Original): A matrix array substrate according to claim 10, wherein said size of the island pattern is substantially equal with a sum of a size of said contact hole and a margin for absorbing deviation of alignment during patterning of said contact hole.